2019

Using All Processor Cores While Being Confident about Timing

Dr. Bjorn Andersson

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Complex, cyber-physical DoD systems depend on correct timing—any timing failure could be disastrous. What's more, while these systems drive demand for use of multicore processors, concern about timing has led to disabling all processor cores except one—limiting system capability.

We aim to develop a solution to overcome this obstacle.

DoD Systems Interact with Their Physical Environment

DoD Systems Include Software






DoD Systems Include Software That Interacts with the Physical Environment






DoD Systems Include Software That Has Real-Time Requirements






Satisfying Real-Time Requirements Is a Challenge for the DoD in General






Satisfying Real-Time Requirements Is Challenging for Upgrading the Blackhawk UH-60 Helicopter






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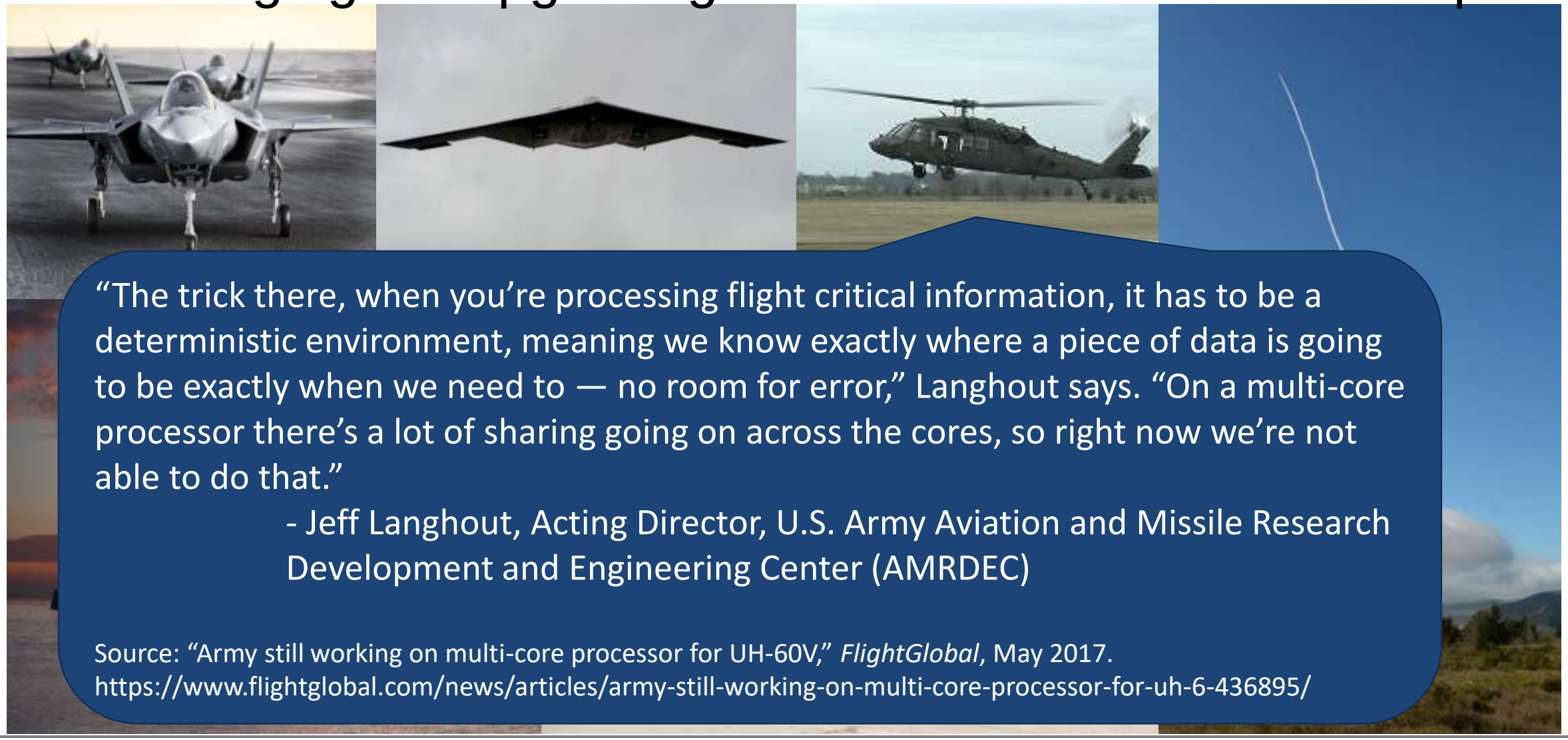
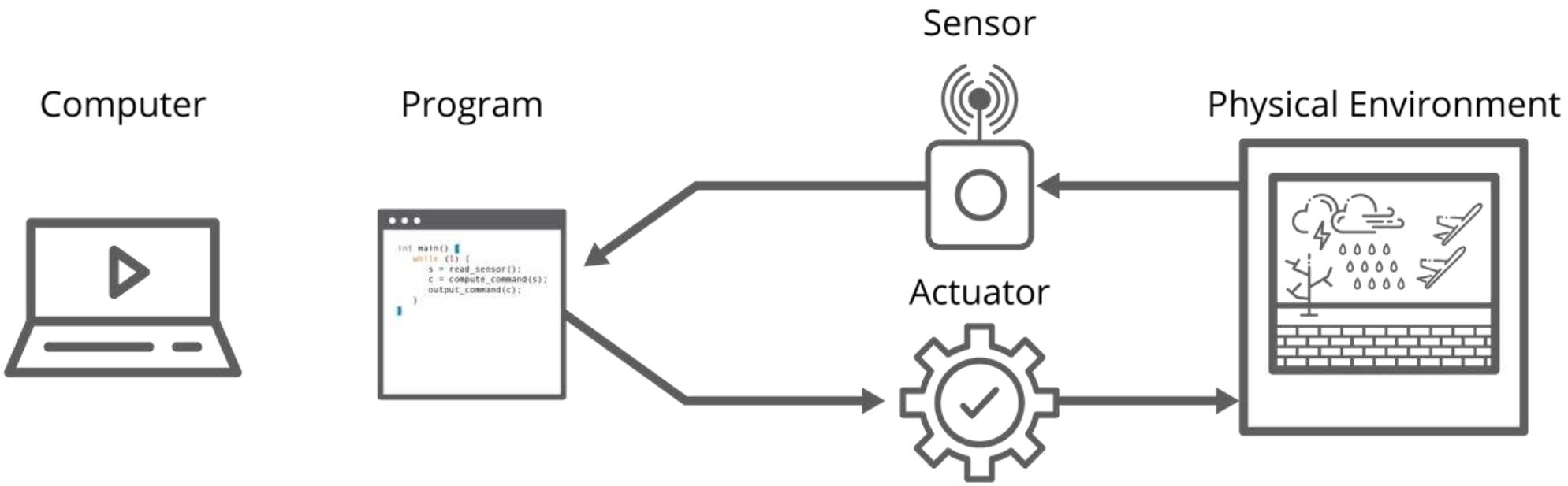


"The trick there, when you're processing flight critical information, it has to be a deterministic environment, meaning we know exactly where a piece of data is going to be exactly when we need to — no room for error," Langhout says. "On a multi-core processor there's a lot of sharing going on across the cores, so right now we're not able to do that."

- Jeff Langhout, Acting Director, U.S. Army Aviation and Missile Research Development and Engineering Center (AMRDEC)

Source: "Army still working on multi-core processor for UH-60V," *FlightGlobal*, May 2017. https://www.flightglobal.com/news/articles/army-still-working-on-multi-core-processor-for-uh-6-436895/

Commonality of DoD Systems



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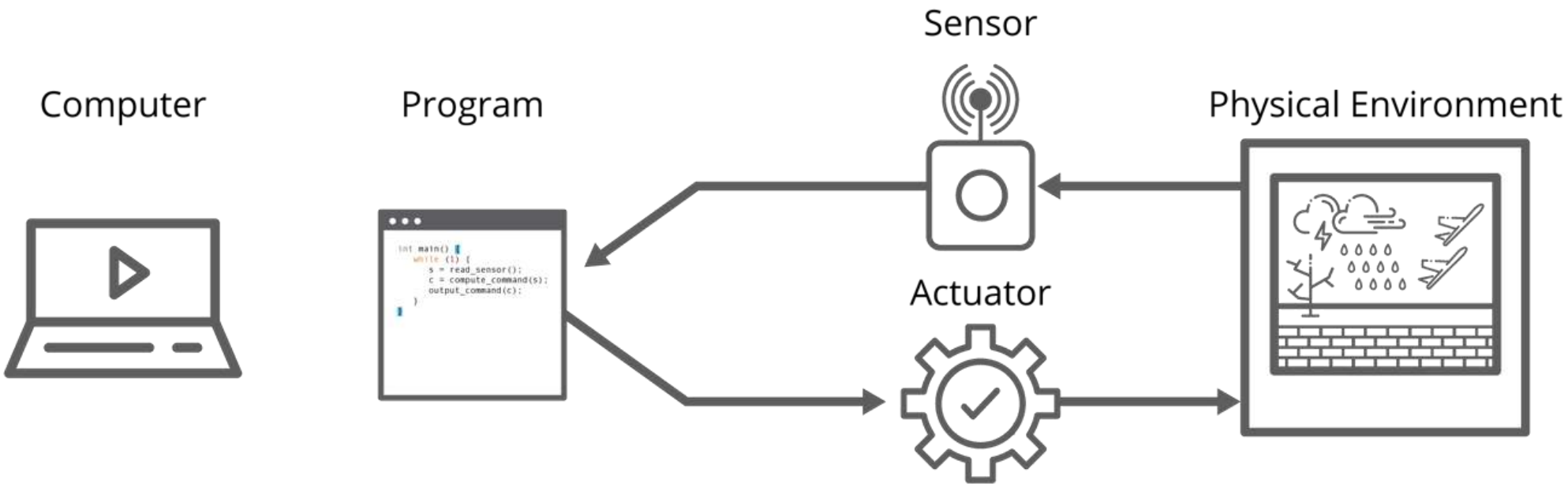

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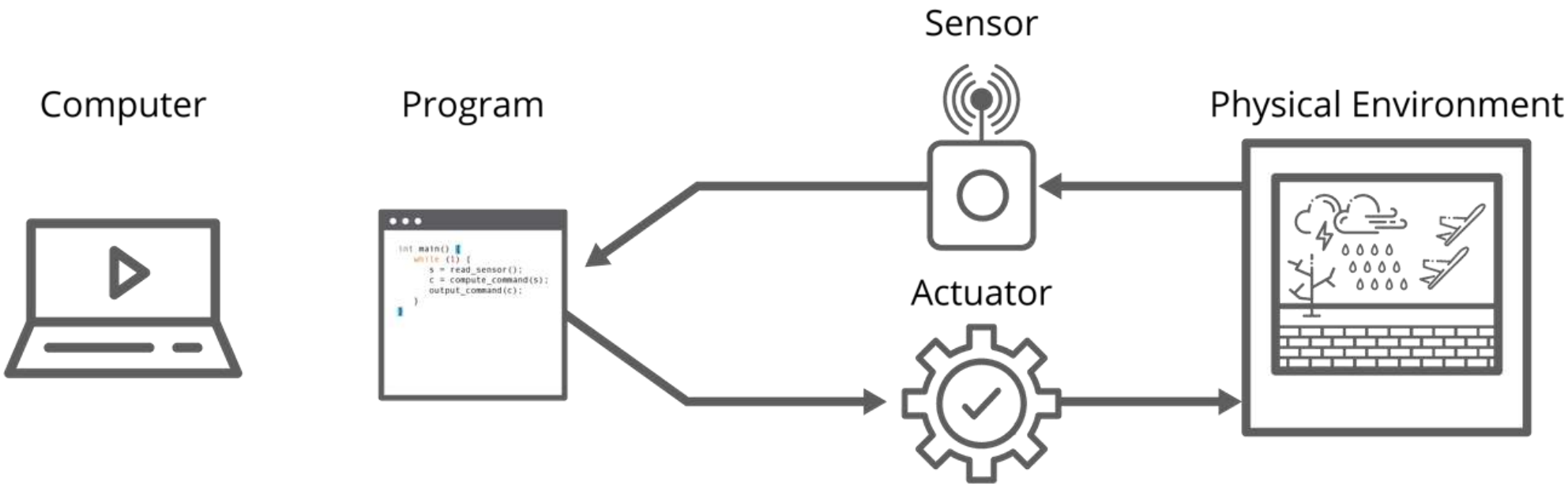

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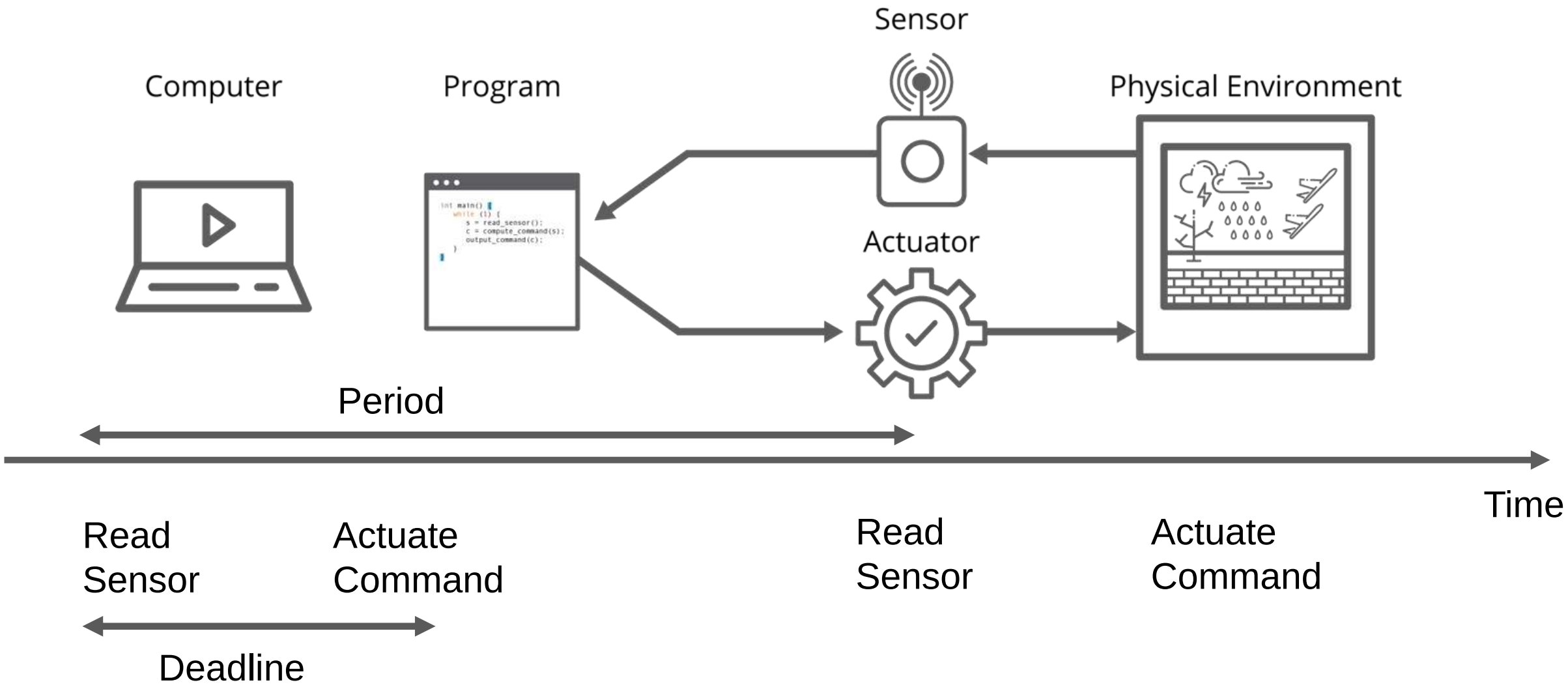

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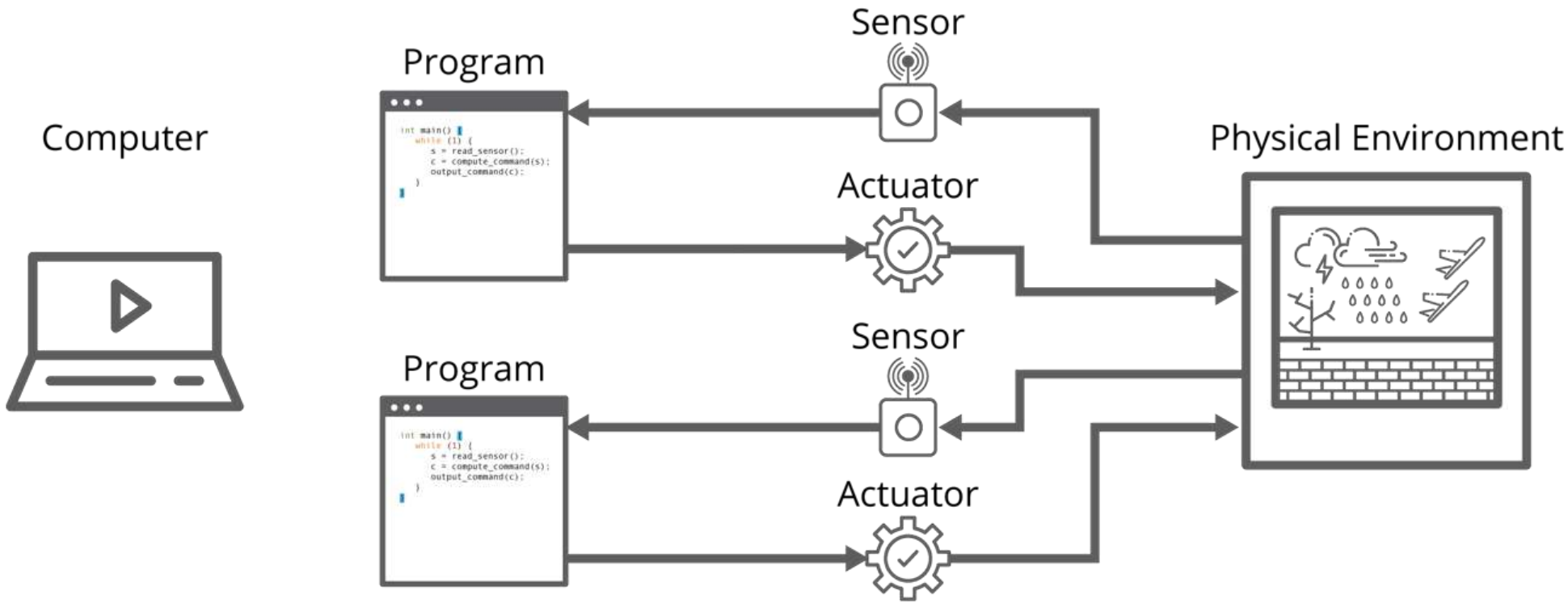

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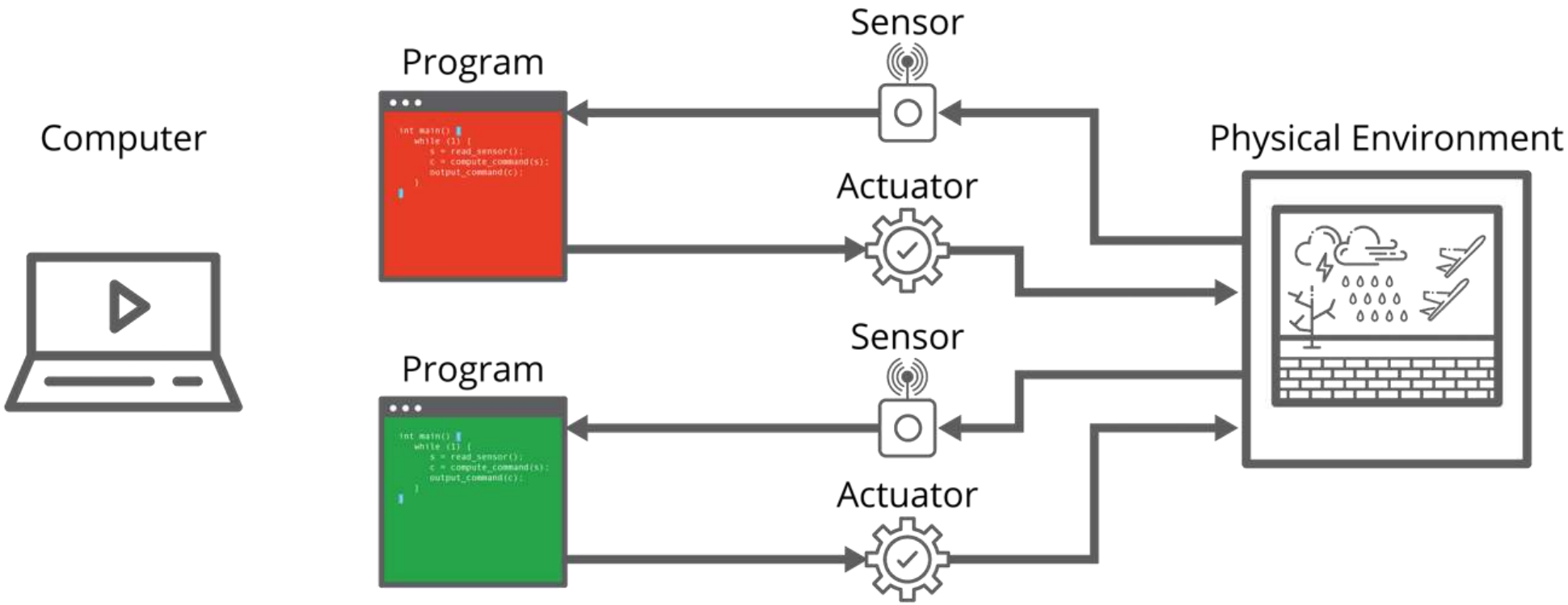

What Makes It Challenging to Satisfy Real-Time Requirements?

What Causes Delay of Software?

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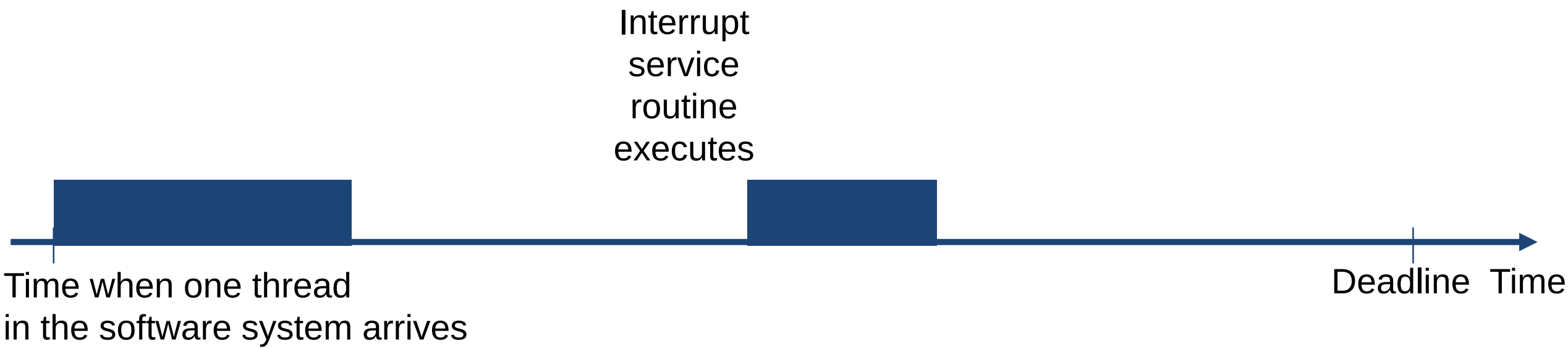

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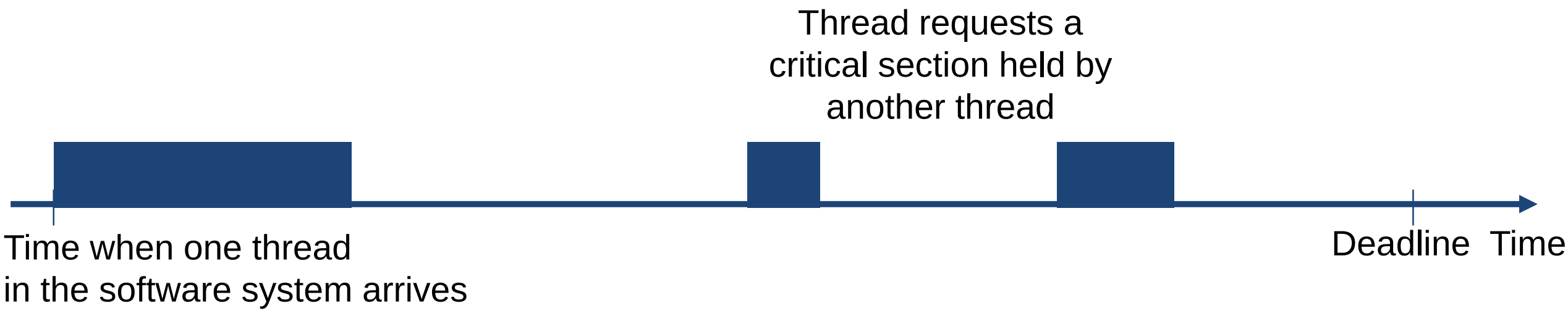
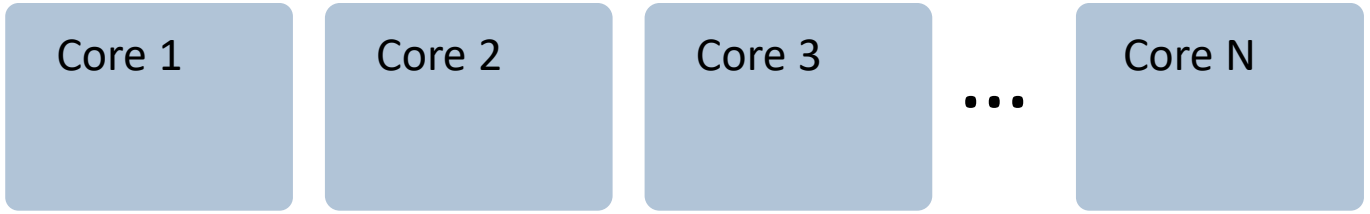


What Causes Delay of Software?

Real-Time Requirements of Software Executing on a Multicore Processor

Hardware Trends

- *All computers are multicores.*



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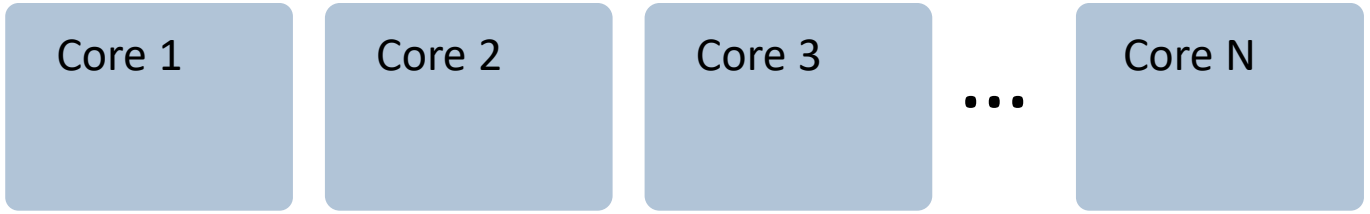

Real-Time Requirements of Software Executing on a Multicore Processor

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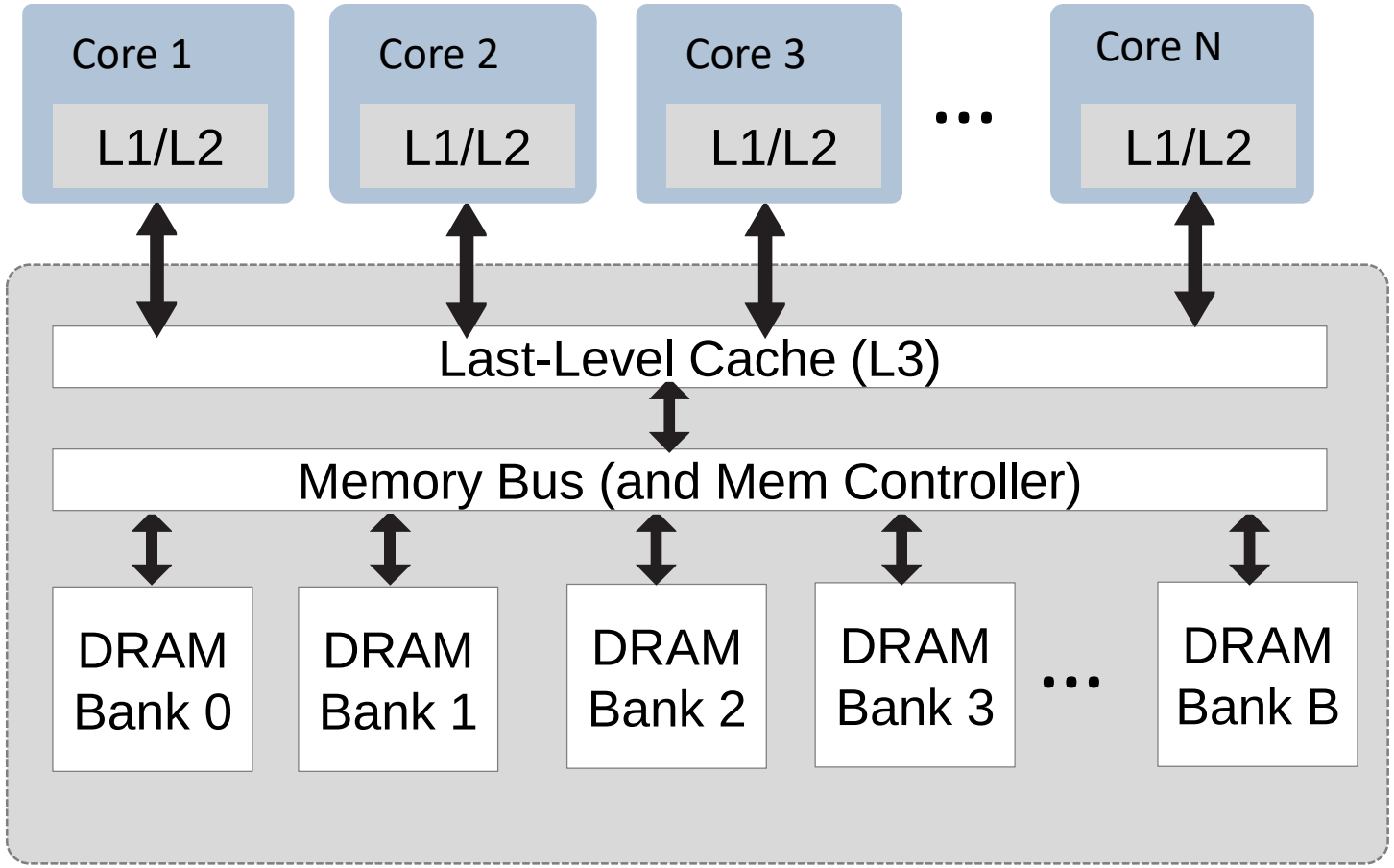
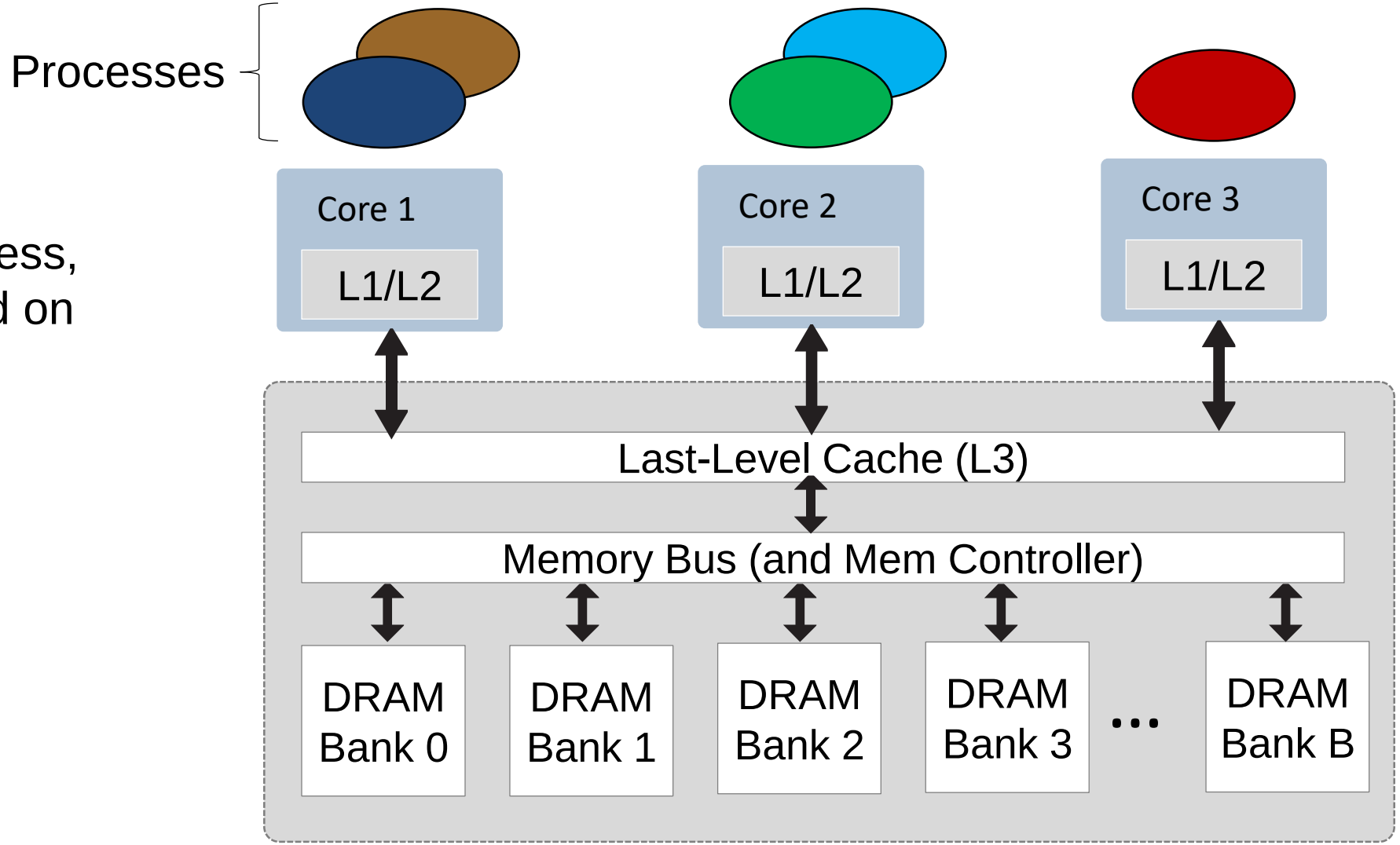
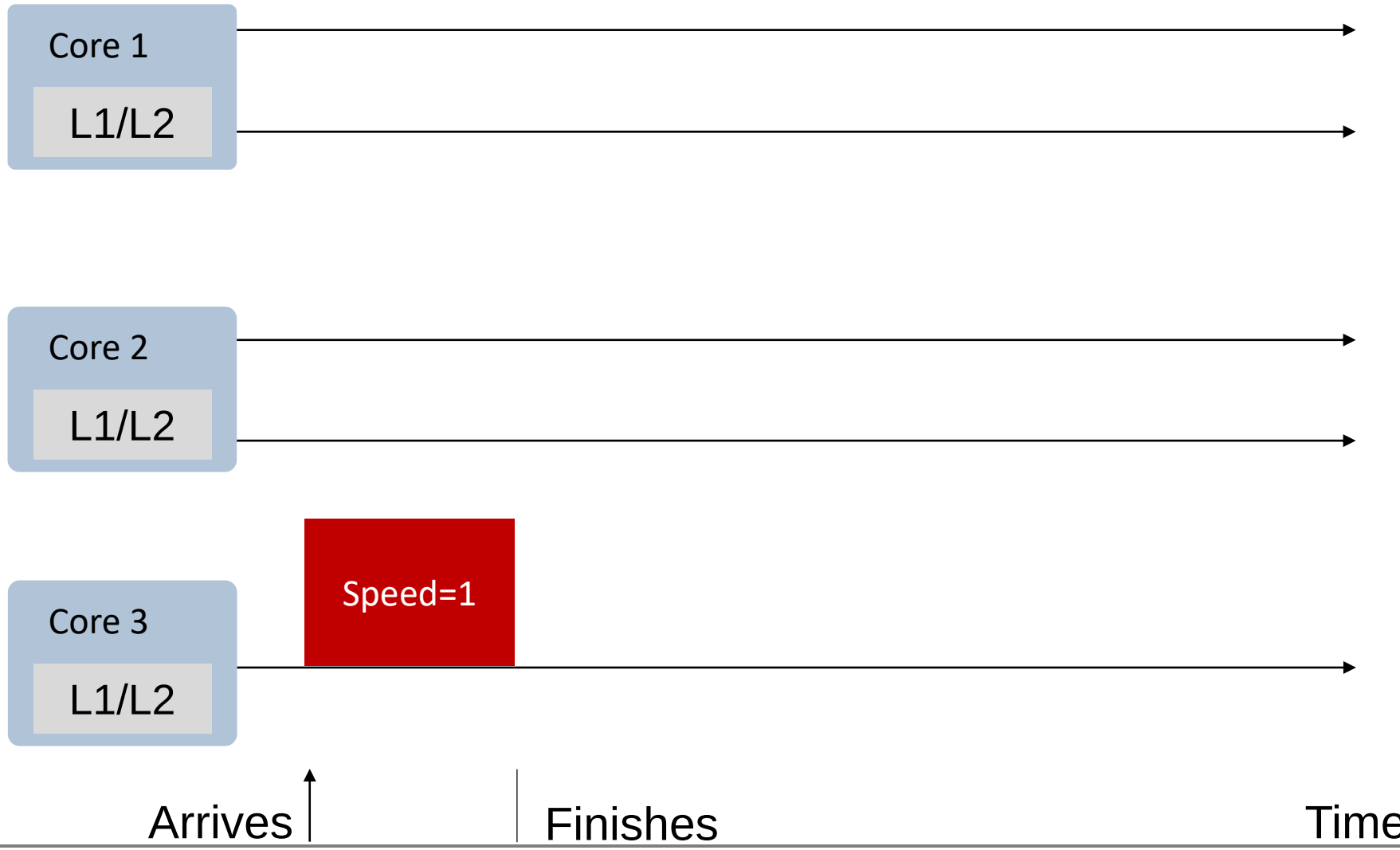
- *Most chip makers do not offer single core.*
- *Most multicores have shared memory.*



Problem: For each process, compute an upper bound on its response time.



How Co-Runners Impact Speed of Execution



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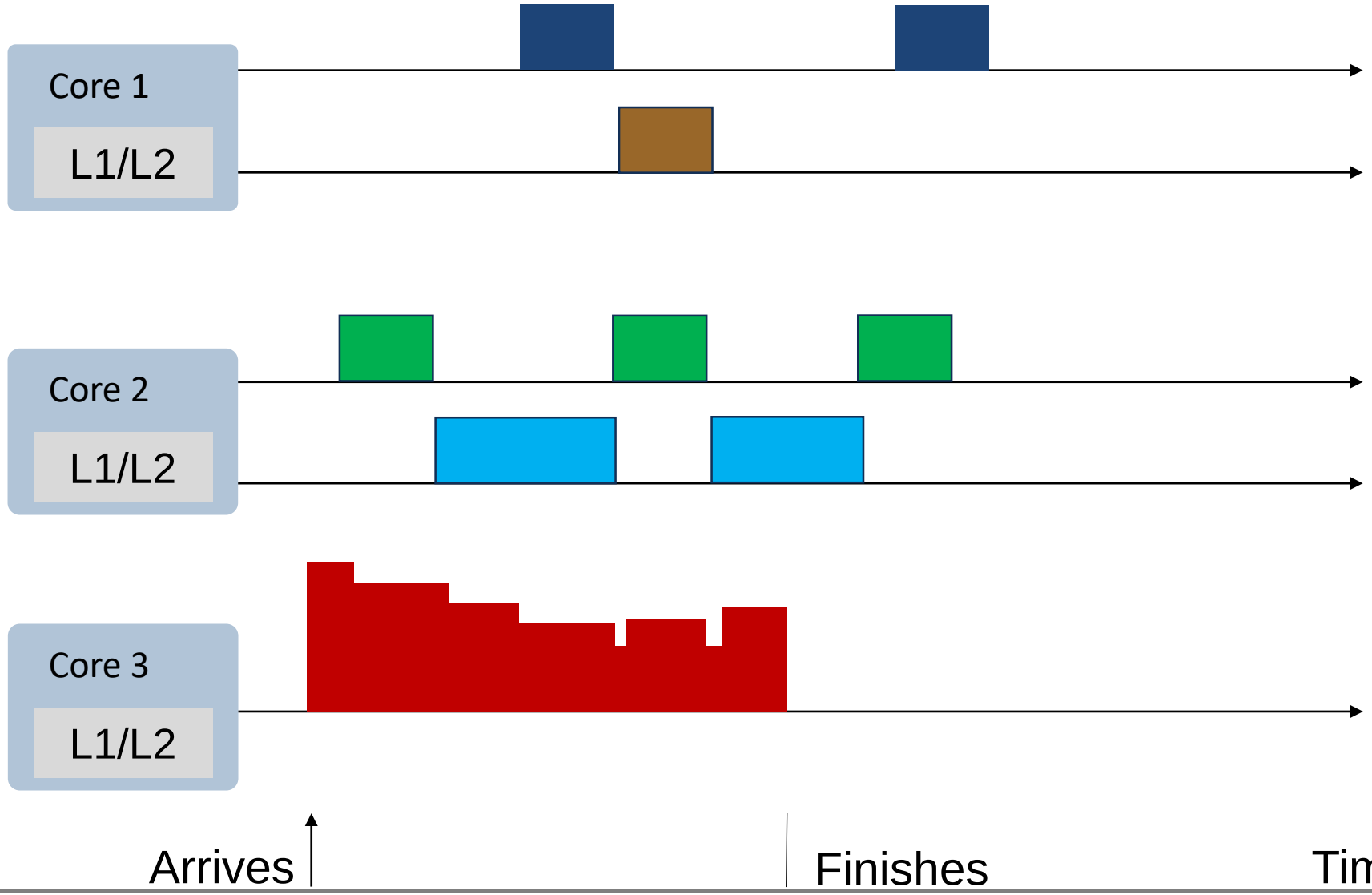

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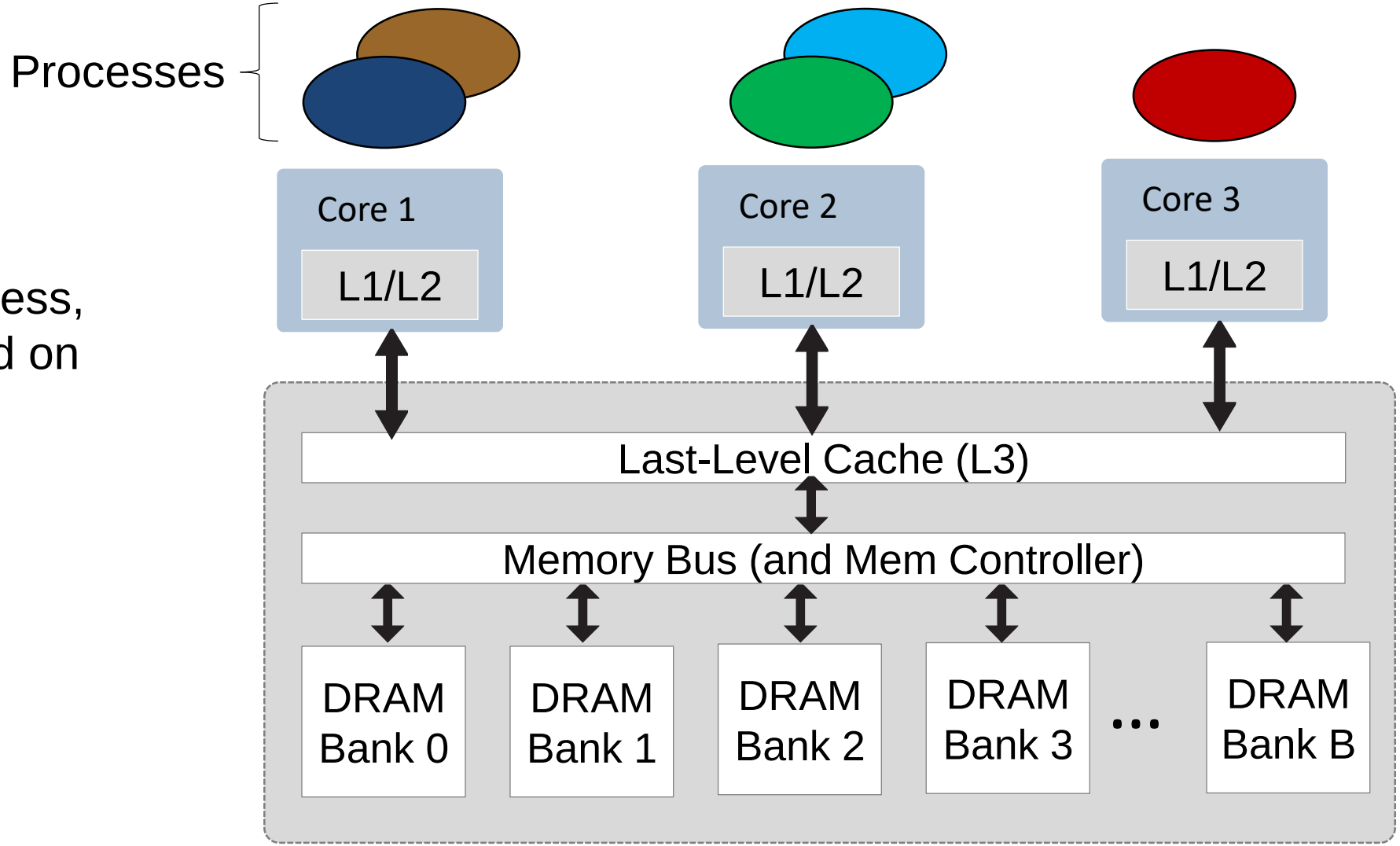

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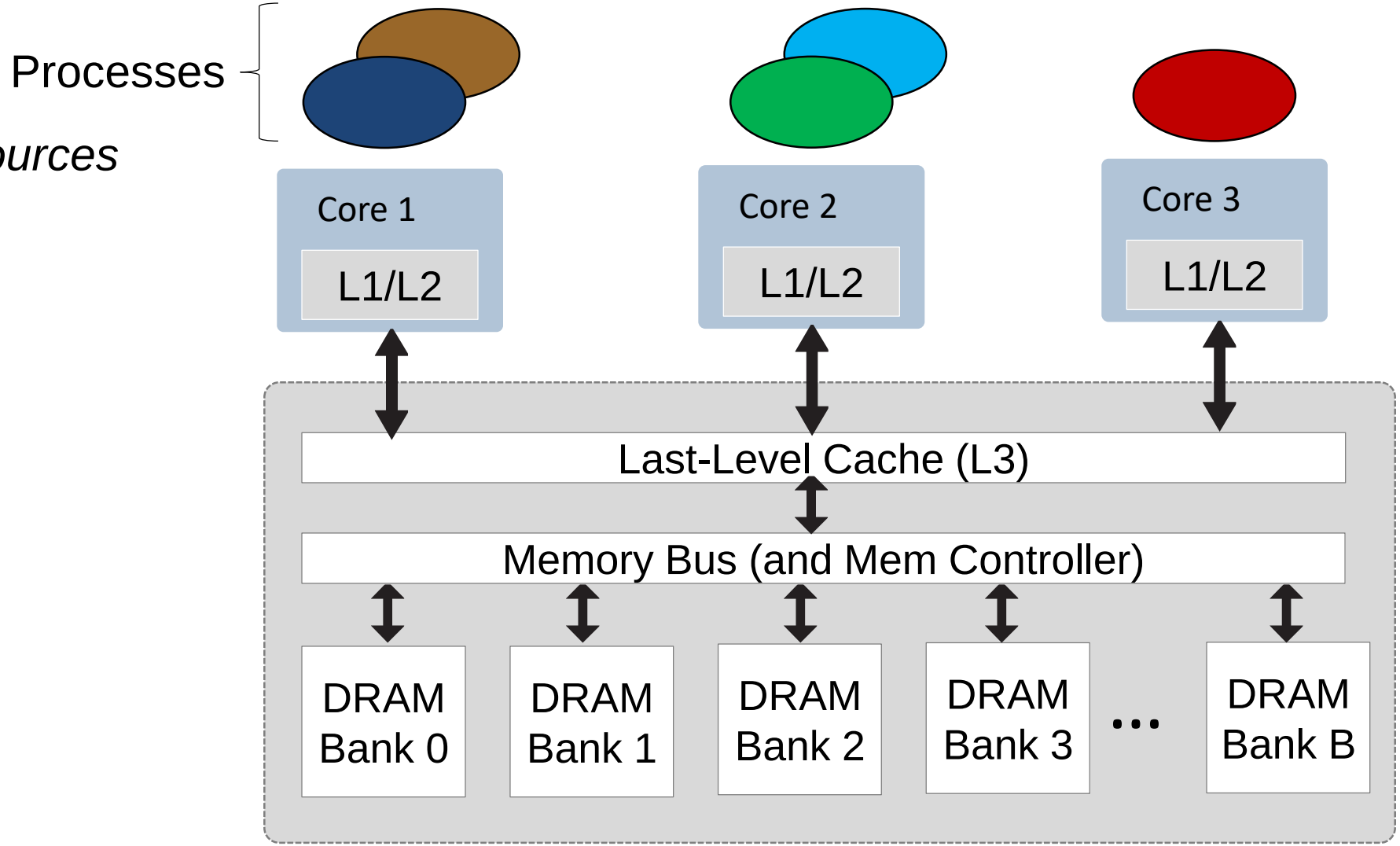

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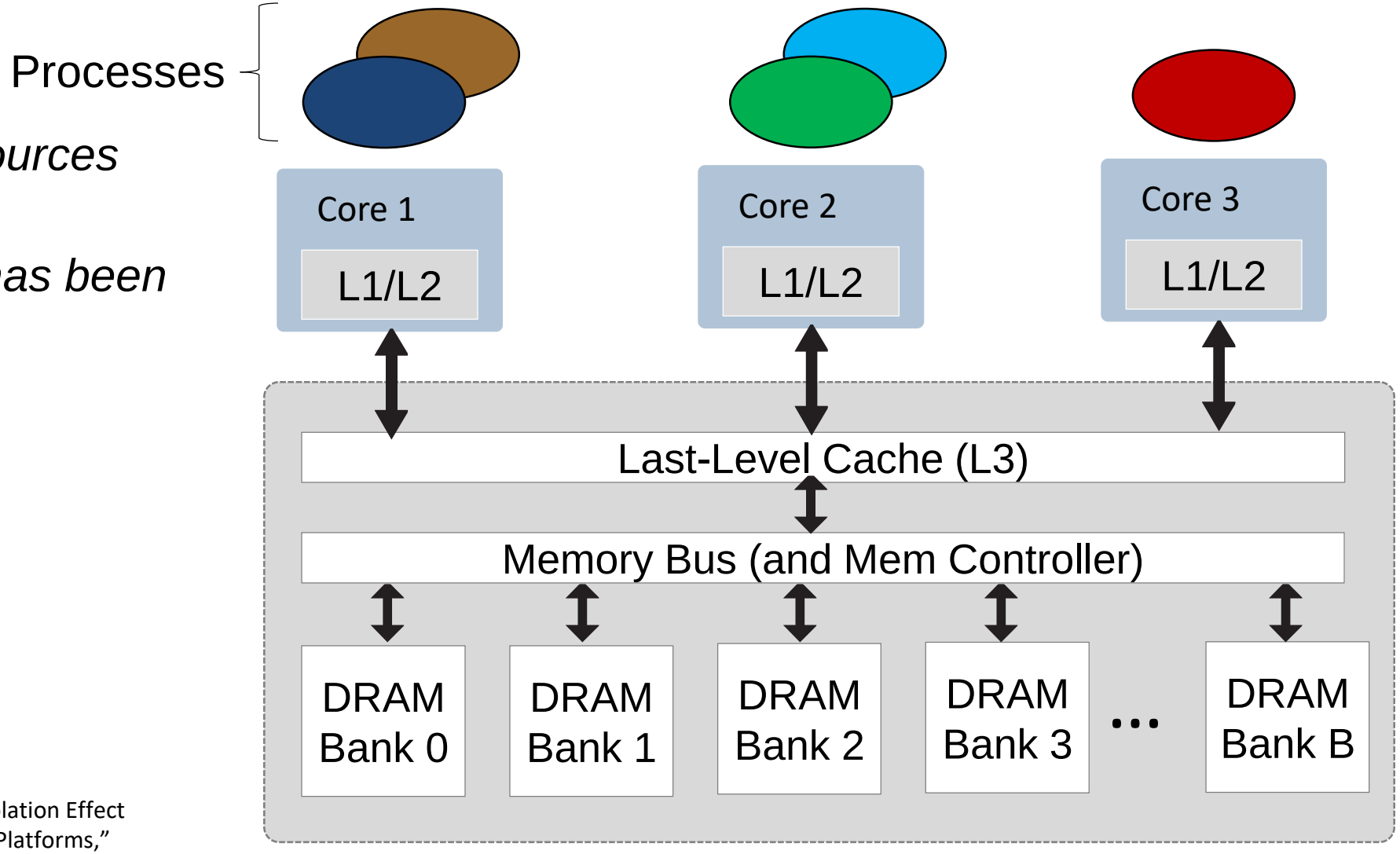

*H. Yun and P. K. Valsan, "Evaluating the Isolation Effect of Cache Partitioning on COTS Multicore Platforms," OSPERT, 2015.

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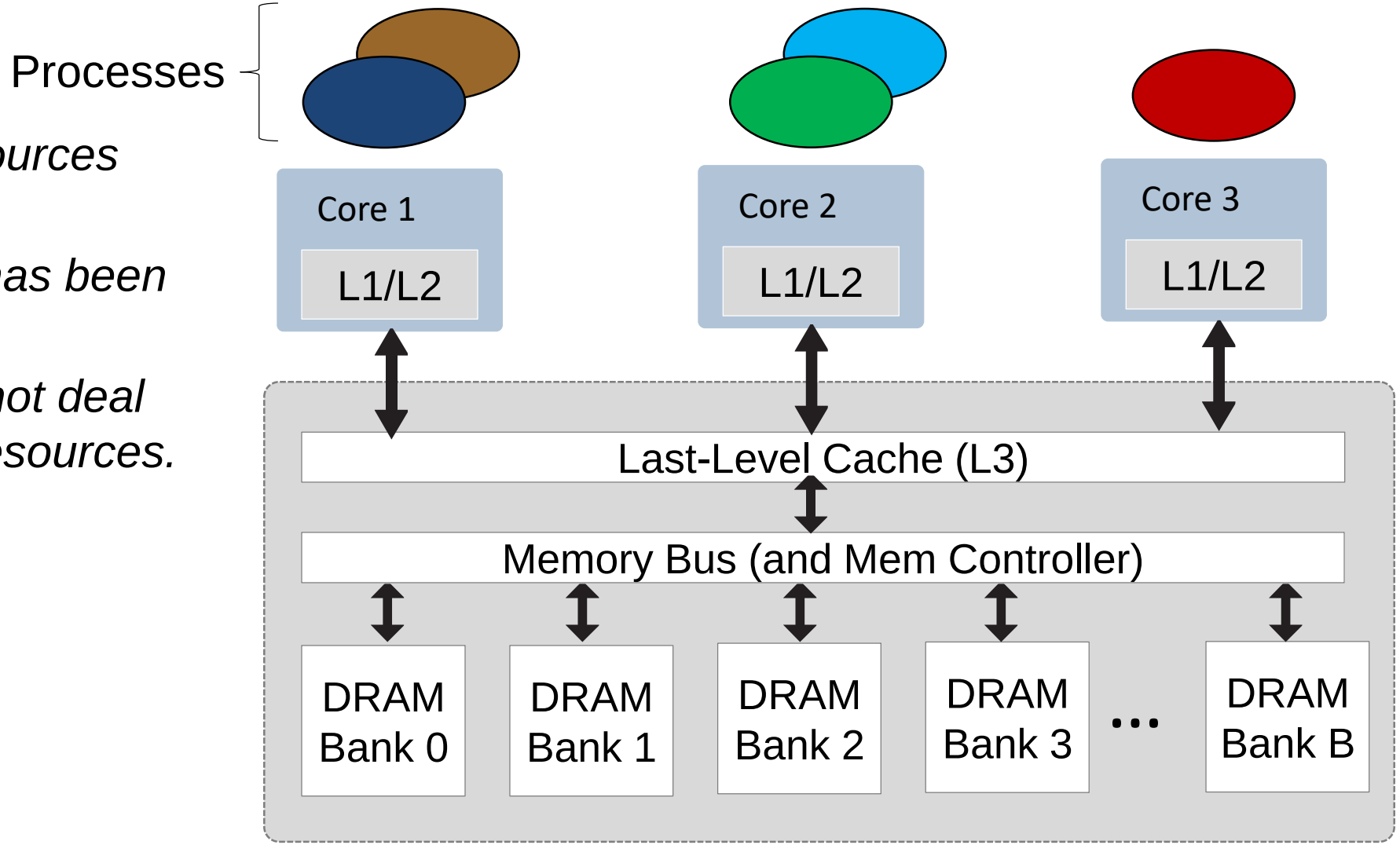

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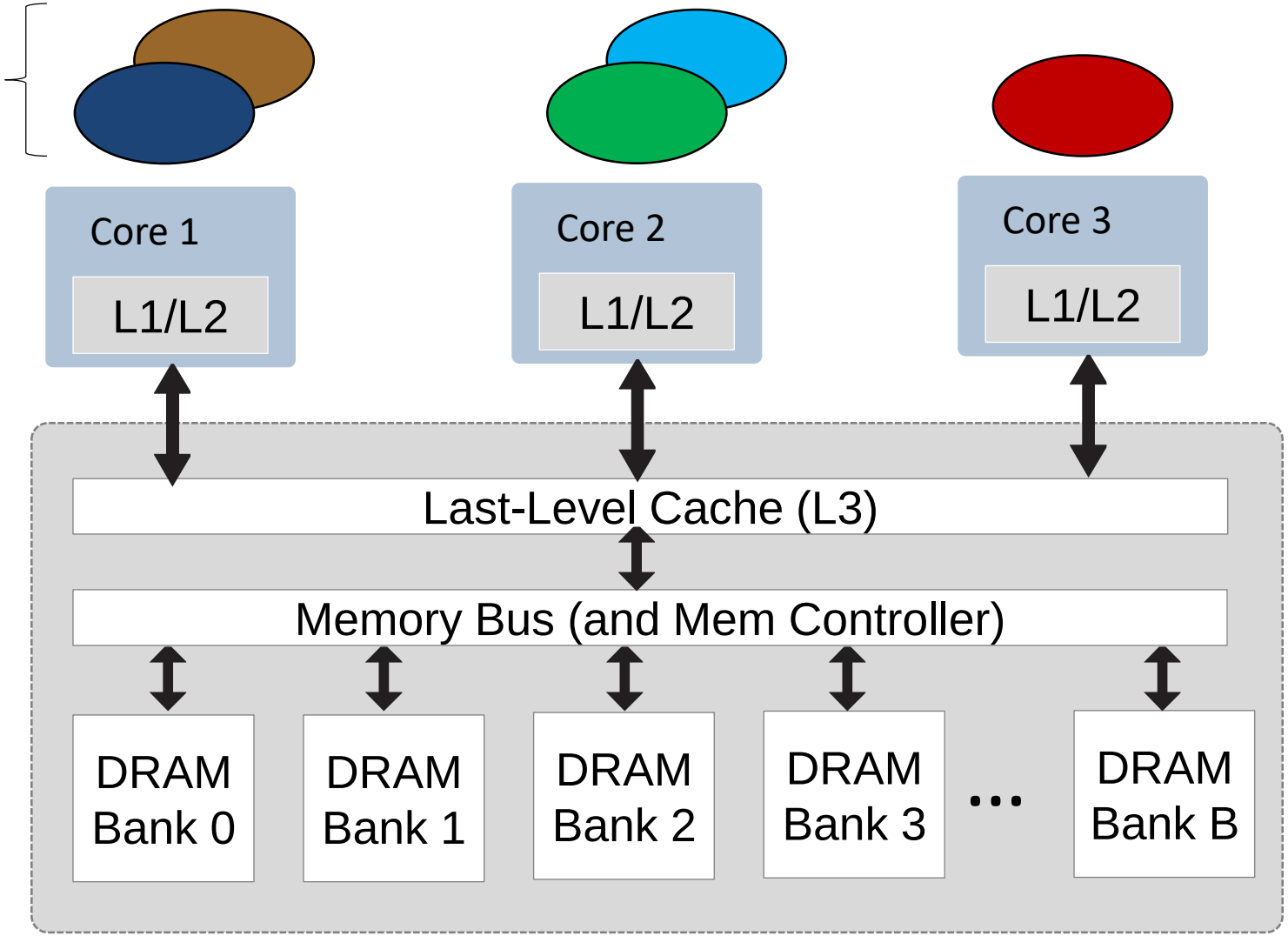

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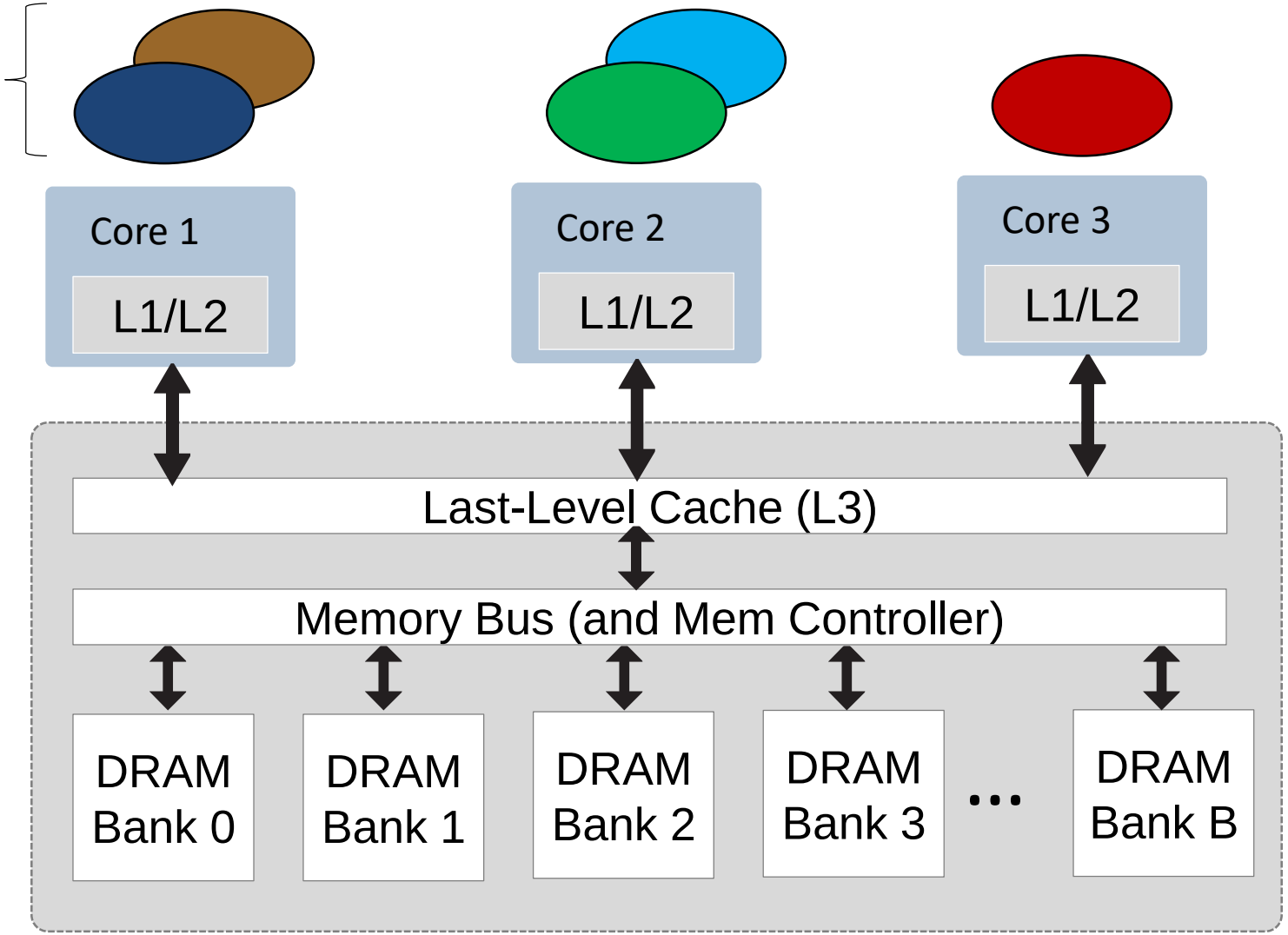

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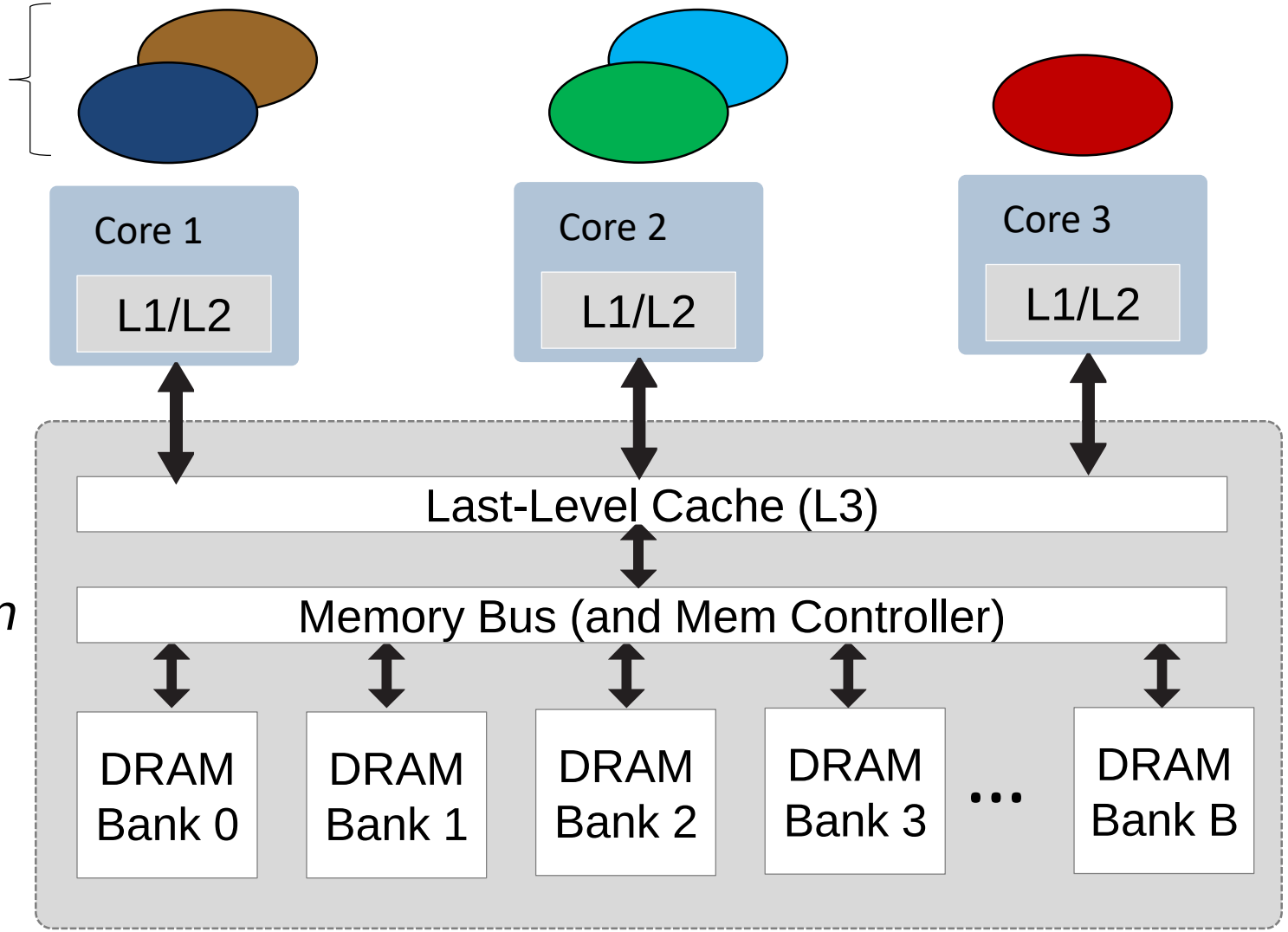


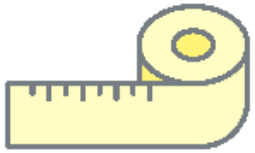
We need a new method to compute response times of processes.

Project Objective

Many real-time systems within the DoD have all processor cores except one disabled in order to be confident about timing.

Therefore, the objective of this project is to develop a solution to overcome this obstacle.

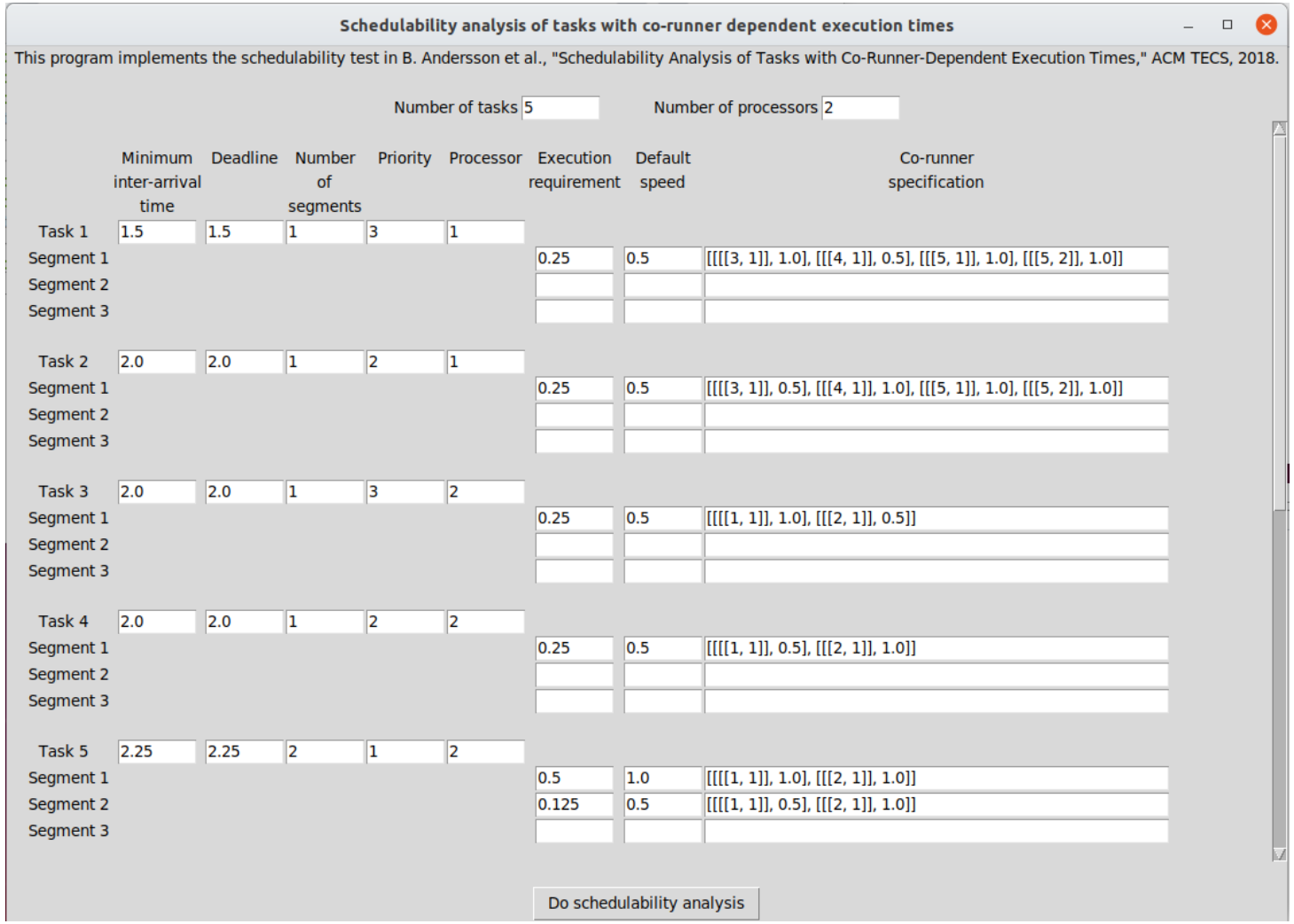
New verification procedure



Method to obtain abstractions

Configuration

A Look at Our Analysis Tool - 1



A Look at Our Analysis Tool - 2