Semiconductor Foundry Verification

Detecting Counterfeit Electronics

Motivation

- Project aims at verifying **history of chip design and manufacturing** used in critical infrastructure.
- Unknown electronic components possess **risk to secure operations.**
- Analysis is done at the integrated circuit (IC) level. Verified information includes **foundry info, design specifics, sources of 3rd party circuitry.**
- **Algorithms detect attribution** with minimal human intervention.

Research Goals

- Well-established algorithmic approach to circuit component recognition based on behavioral matching of an unknown sub-circuit against a library of abstract components
- Leverage available component/foundry information to study the attribution impact and extract samples of sub-circuits.
- Measure logic gate density, metal layer routing, collections of logic gates.
- Analyze numerous different ICs for differentiating factors.
- Verify results on another relatively large set of various ICs.

Main Idea

- Semi-automated image processing to detect chip features
- Each layer is photographed and processed
- Relevant features extracted and checked against rules
- Fabrication facilities have design and fabrication requirements and tolerances

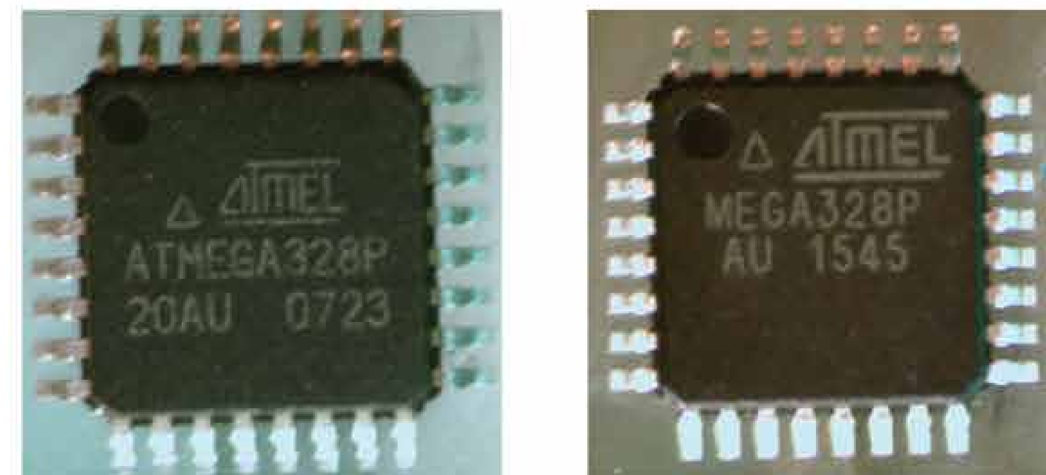
Some potential examples fabrication requirements:

- No acute angles or angles of non-45 degree integer multiples
- All metal feature sizes must be multiples of X nm
- Metal layers will be copper

Failure to meet these rules flags chips as potential counterfeits

Experimental Results

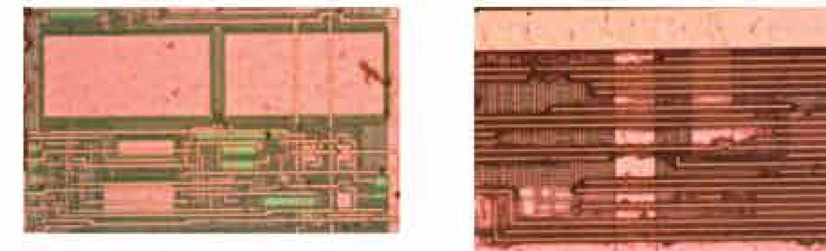
Counterfeit Examples. These two chips appear to be identical. The one on the left is counterfeit, the one on the right is authentic.



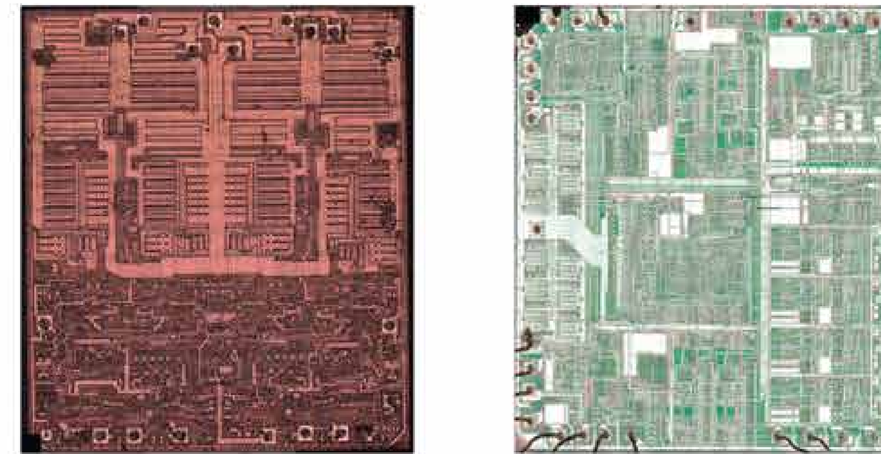
Integrated Circuit Fabrication

- Doping agents, glasses, or metals on silicon
- Individual components nowadays are on the order of 100nm~10nm
- Chips are multi-layered • Bottom layer is transistors, other silicon features
- Layers above alternate:
  - Metal interconnects (copper/aluminum)
  - Vias (same material as metal)
  - Glass (Silicon Dioxide) between all of this, isolating the layers
- Topmost layer contains pads for connecting to packaging and an encapsulation layer

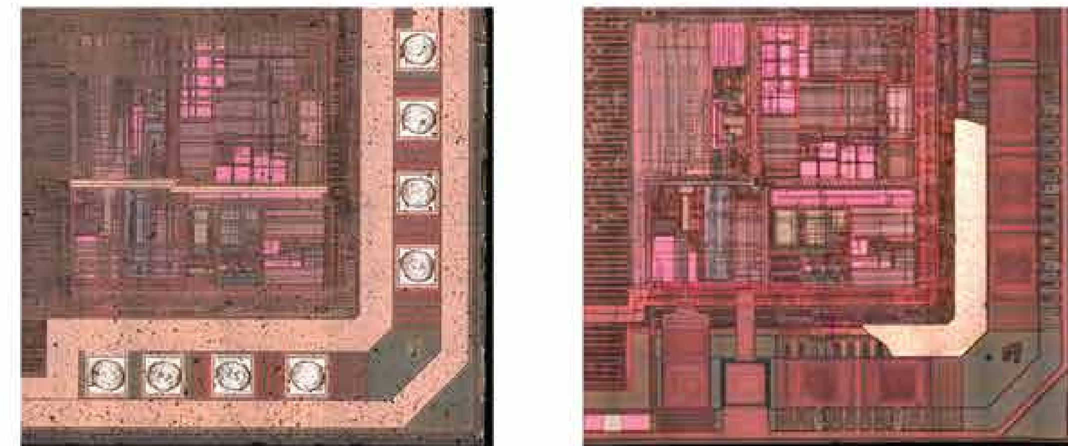
Same Foundry



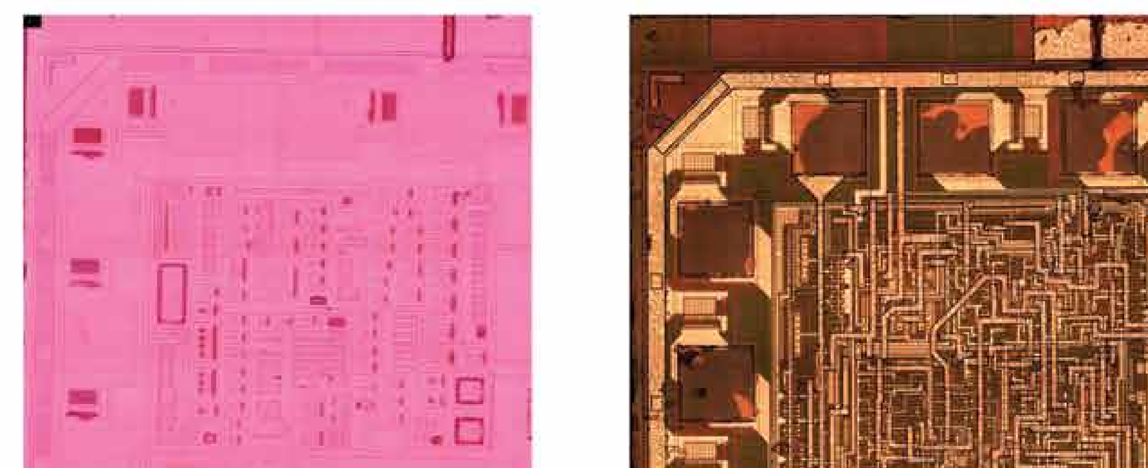
Different Foundries



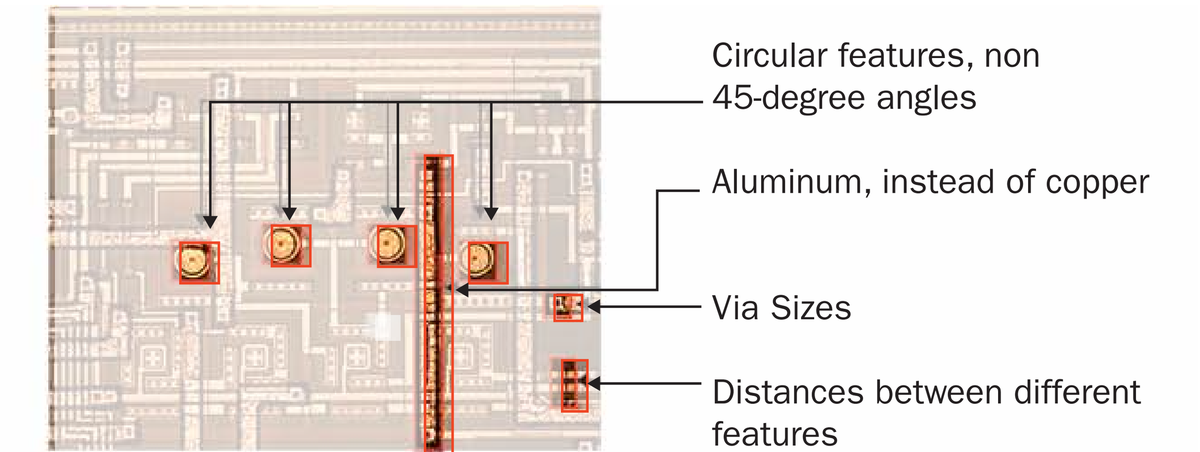
Authentic Chip Delayered. The process exposes additional features in layers below. Pads, metals and via sizes, distances between features and the edge of the die indicate manufacturing process and requirements of a specific foundry.



Counterfeit Chip Delayered. Similar process for counterfeit chip reveals features that are very different from the manufacturing process used in authentic IC.

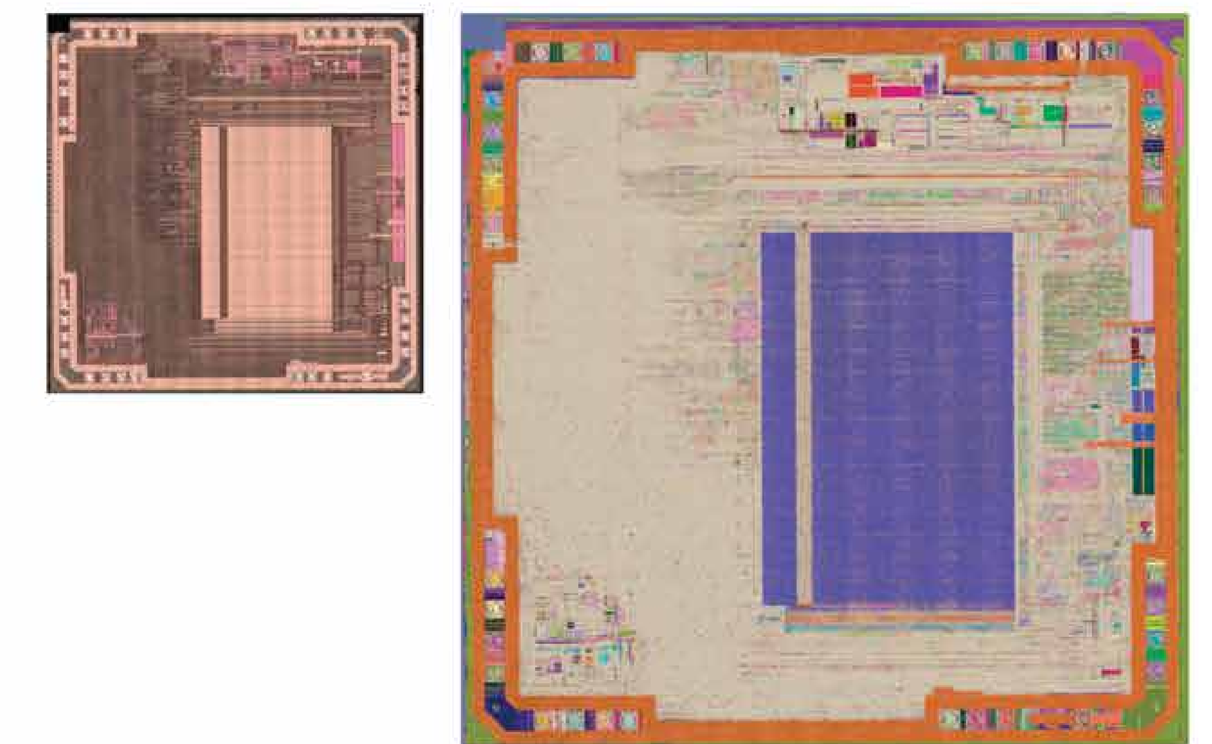


Important Manufacturing Differences



Project Outcomes

Automated Analysis Framework.Square Area Density Based Spacial Cluster Analysis with Noise (SADBSCAN)



- Method of cluster analysis specifically designed for segmentation and area differentiation in images
- Weights the geographical difference as more important and mark these objects as different clusters
- Queries different regions separately and efficiently
- Calculates simple Euclidian distance of color values
- Combines clusters of pixels based not only on color similarities but also the “geographic” location
- Accurate feature detection with high speed parallel processing (10-15 minutes on 1GB image)
- Various additional analytical image processing and feature extraction methods implemented in plugins

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